A LOW COST 3.6V SINGLE-SUPPLY GaAs POWER AMPLIFIER IC FOR THE 1.9-GHz DECT SYSTEM

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ABSTRACT

A GaAs power amplifier IC in a SOIC-16 plastic package has been developed for the 1.9 GHz Digital European Cordless Telephone (DECT) system. The power amplifier consists of two stages with all matching structures on chip and has a total area of 1.84 mm^2. At -2 dBm input power and 3.6 volts, the typical power amplifier achieves 26 dBm output power with 30% power-added efficiency, while operating from a single power supply in the SOIC-16 plastic package.

INTRODUCTION

Commercial GaAs MMIC's for wireless applications are under active development in the microwave industry. Previous designs [1,2,3,4,5] have demonstrated excellent performance at the expense of high system integration and packaging costs.

The present work describes a power amplifier designed for the 1.88 to 1.90 GHz Digital European Cordless Telephone (DECT) frequency band with a specific goal for cost minimization. The targeted areas for cost minimization are:

1. Minimization of chip size.
2. Use of low cost packaging.
3. Minimize system parts count.

The key element for achieving a low cost design requires understanding the DECT system requirements. The Gaussian Frequency Shift Keying (GFSK) modulation format used in DECT is a constant envelope signal enabling the use of non-linear amplification. The power output at the antenna is constant and limited to +24 dBm. The classical approach utilizing Class-AB or B amplification can be used, however the added cost of negative voltage required for typical GaAs MESFET implementation is highly undesirable. The DECT system incorporates Time Division Duplexing (TDD) which allows 12 users to share the same channel. The transmit timing for DECT requires a 416 μs period with a 4% duty cycle. This requires the transmitter to be fully turned-off (> 40 dB) between pulses and to have low leakage current to minimize the battery drain.

IC FABRICATION PROCESS

The ITT MSAG-Lite ® process is a streamlined version of the MSAG process [6,7] that was used for this product design with only 8 masking levels required. The process features a 0.6 μm self-aligned Titanium Tungsten Nitride (TiWN) gate that provides excellent yield and reliability. On 4-inch wafers, the percent deviation (1σ/mean wafer-to-wafer) of current and threshold is typically 9%. Circuit interconnects are made using 4.5 μm thick Gold plating which is essential for low loss matching networks at the PCS frequencies. The entire circuit is protected by a scratch protection polyimide layer to improve assembly yield in the high volume packaging environment. The processed wafers are thinned to 125 μm to reduce thermal resistance.

Despite it's simplicity, the MSAG-Lite process offers state-of-the-art power performance. The 3G FET (optimized for 3V drain bias operation) that was used for this design has a RF output power density of 200 mW/mm, MAG of 18 dB at 2 GHz and a high f_T of 19 GHz. To generate high power-added-efficiency at 3 V drain bias, the 3G FET was designed with a high peak saturated drain current (300 mA/mm) and a relatively low knee voltage (Vk = 0.5 V at IDSS). The typical two-terminal breakdown voltage is greater than 9 V @ 1 mA/mm. At zero gate bias, the saturation current is 1/2 the peak current. The 3G FET can safely operate at IDSS so the gate voltage can be applied after the drain voltage without damaging the IC.

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CIRCUIT DESIGN

In order to compete with silicon with respect to cost, the typical requirement for GaAs using a negative gate supply must be eliminated. The IDS-VGS curve for the 3G FET is shown in Figure 1. With 0 volts applied to the gate, the signal swing is symmetrical about IDSS. By operating grounded gate, a Class-A power amplifier is obtained. Table 1 shows the device load-pull data in Class-A operation tuned for maximum power. This amplifier when operating compressed will meet the requirements for the DECT system shown in Table 2 without the requirement for negative gate bias.

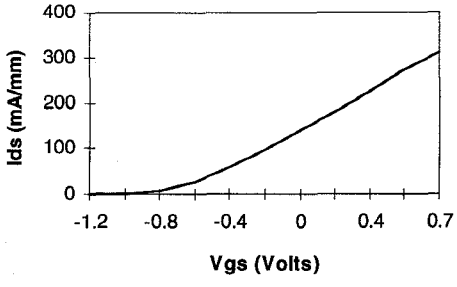

Figure 1.MSAG-Lite®: IDS vs VGS @ VDS=3.0V

The requirement for good efficiency and output power resulted in selecting the 300 um FET for the first stage and a 2.4 mm FET for the second stage. ITT user-defined large signal models were developed from small signal S-parameters, pulsed I-V and load-pull measurements. The DECT MMIC incorporates on chip input and output matching which added ~30% to the MMIC area, but the design still meets cost and system requirements. Inductive, pi and low-pass matching circuits were used for the input, interstage and output matching circuits respectively. The final chip size is 1.08 mm X 1.70 mm The schematic for the DECT MMIC is shown in Figure 2 and the MMIC layout is shown in Figure 3.

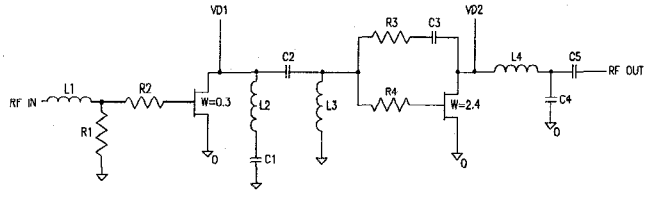

Figure 2. DECT MMIC Schematic

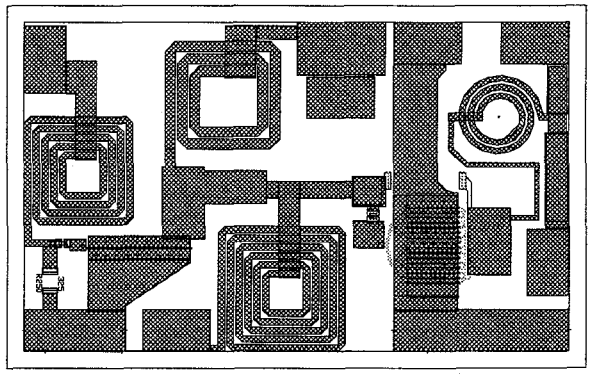

Figure 3. DECT MMIC

The final requirement is to design a simple, low cost method to pulse the amplifier and maintain rise and fall times shown in Table 2. By using a MOSFET switch, the drain voltage can be turned on and off with CMOS level signals. A series resistor added to the MOSFET gate for pulse timing was optimized using SPICE. The total leakage current in the off-state is less than 1 μA enabling long battery life between transmissions.

INPUT POWER (dBm)	POWER OUT (dBm)	mw/mm	PAE (%)
-15	4.8	1.3	0.3
-10	9.8	4	0.8
-5	14.8	12.7	2.9
0	19.9	41	9.6
5	24.5	118	28
10	26.4	184	44
15	27.3	224	51

2.4 mm FET, 3.0 VDC, Class -A Bias, 1.85 GHz
TABLE 1.

Conditions:	
Frequency Range	1.88 to 1.9 GHz
Supply Voltage	3.6 VDC
RF Input Power	-2 dBm
Temperature (PIN 4)	25 C
Requirements:	
Power Out	26±1 dBm
Current with Pin = -2 dBm	≤420 ma
Input VSWR	≤ 2.0:1
Gain Variation in Band	0.5 dB
Pulse Rise/Fall Time	1 to 10 usec
Power Out On/Off	≥ 40 dB
Operating Temperature (PIN 4)	-10 to 65 C

Basic DECT Power Amplifier Requirements
Table 2.

During pulse operation, the VCO that drives the power amplifier can be pulled off frequency if the power amplifier input VSWR changes abruptly. A by-product from picking the compressed Class-A amplifier and pulsing the drain is the minimization of the input VSWR between the amplifier's on and off states. Since the input FET gate bias is fixed at 0 V, VCO loading is minimized.

For system integration, the DECT power amplifier requires no external matching components. A MOSFET switch with a timing resistor is required for pulse operation. Since a SOIC-16 package was selected, the two RF chokes and by-pass capacitors must be added at the circuit assembly level. The RF chokes may be either wire-wound or printed. The complete DECT power amplifier schematic with the timing circuit is shown in Figure 4.

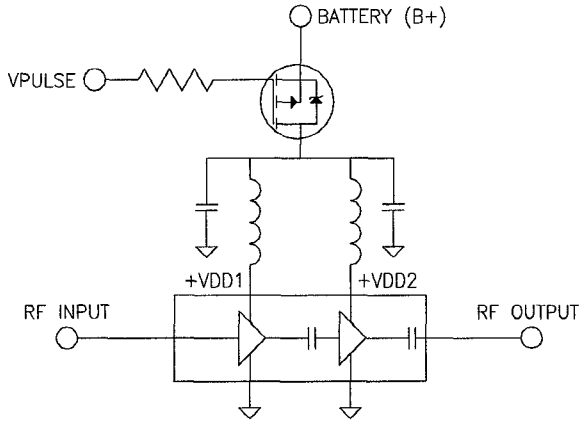

Figure 4. DECT Amplifier with Timing Circuit

MEASURED PERFORMANCE

Measured performance for the DECT power amplifier with a -2 dBm input signal shows 26 dBm power out with a PAE of 30% as shown in Figure 5. Over the full range of process fabrication variation in IDSS the output power varies only ±0.25 dB and the PAE changes only ±4 points. The input VSWR shows little change due to process variations. The -2 dBm input compresses the amplifier ~1.5 dB. The PAE can be improved to 33% by driving the power amplifier with 0 dBm. Due to Class-A operation and the low-pass output match, this amplifier utilizes no harmonic filtering. With -2 dBm input, the second harmonic is -33 dBc and third harmonic is -40 dBc.

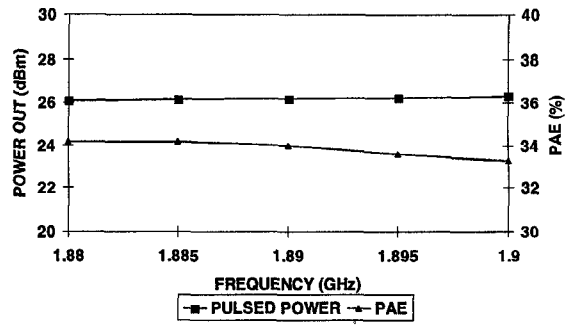

Figure 5. Pulsed Power and PAE

The pulse wave form for the detected power out is shown in Figure 6. This easily fits between the 1 and 10 us rise and fall time requirements for DECT.

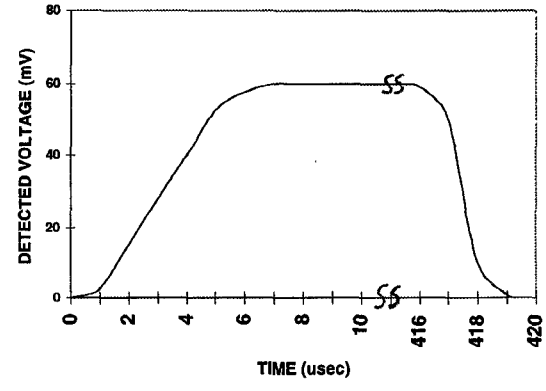

Figure 6. Detected RF Output Power

CONCLUSION

The design and test results of a 1.9 GHz GaAs power amplifier IC in a plastic SOIC-16 package has been described in this paper. The small size, performance and simple system integration make it a suitable choice for insertion in DECT systems.

ACKNOWLEDGMENTS

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